Listing of Claims:

Please amend the claims as follows. This claim set is to replace all prior versions.

1 - 2. (Canceled)

3. (Currently amended) ~~The memory interface system of Claim 2,~~ A memory interface system, comprising:

at least one channel line that couples a memory to a memory controller, the at least one channel line being responsive to a terminal voltage that is independent of a memory supply voltage and a memory controller supply voltage;

wherein the memory comprises a first transmitter and a first receiver, the memory controller comprises a second transmitter and a second receiver, and the at least one channel line comprises a first channel line that couples the first transmitter to the second receiver and a second channel line that couples the second transmitter to the first receiver; and

wherein the first and second receivers are powered by the memory supply voltage and the memory controller supply voltage, respectively.

4. (Original) The memory interface system of Claim 3, wherein the first and second transmitters are operable independent from the memory supply voltage and the memory controller supply voltage, respectively.

5. (Currently amended) The memory interface system of Claim ~~2~~ 3, further comprising:

a first level shifter circuit that couples the second channel line to the first receiver; and a second level shifter circuit that couples the first channel line to the second receiver.

6. (Currently amended) The memory interface system of Claim ~~2~~ 3, wherein the first and second transmitters respectively comprise first and second open-drain MOS transistors.

7. (Currently amended) The memory interface system of Claim ~~2~~ 3, wherein the first and second receivers respectively comprise first and second differential amplifier circuits.

8. (Original) The memory interface system of Claim 7, wherein the first differential amplifier circuit is responsive to a first reference voltage and a data signal carried on the second channel line, and wherein the second differential amplifier circuit is responsive to a second reference voltage and a data signal carried on the first channel line.

9. (Original) The memory interface system of Claim 7, further comprising:

a first level shifter circuit that couples the second channel line to the first differential amplifier circuit; and

a second level shifter circuit that couples the first channel line to the second differential amplifier circuit.

10. (Currently amended) The memory interface system of Claim ~~1~~ 3, wherein a magnitude of the terminal voltage is greater than magnitudes of the memory supply voltage and the controller supply voltage, respectively.

11 - 12. (Canceled)

13. (Currently amended) ~~The data processing system of Claim 12,~~ A data processing system, comprising:

a memory that is responsive to a memory supply voltage;

a memory controller that is responsive to a memory controller supply voltage; and at least one channel line that couples the memory to the memory controller, the at least one channel line being responsive to a terminal voltage that is independent of the memory supply voltage and the memory controller supply voltage;

wherein the memory comprises a first transmitter and a first receiver, the memory controller comprises a second transmitter and a second receiver, and the at least one channel

line comprises a first channel line that couples the first transmitter to the second receiver and a second channel line that couples the second transmitter to the first receiver; and

wherein the first and second receivers are powered by the memory supply voltage and the memory controller supply voltage, respectively.

14. (Original) The data processing system of Claim 13, wherein the first and second transmitters are operable independent from the memory supply voltage and the memory controller supply voltage, respectively.

15. (Currently amended) The data processing system of Claim ~~12~~ 13, further comprising:
a first level shifter circuit that couples the second channel line to the first receiver; and
a second level shifter circuit that couples the first channel line to the second receiver.

16. (Currently amended) The data processing system of Claim ~~12~~ 13, wherein the first and second transmitters respectively comprise first and second open-drain MOS transistors.

17. (Currently amended) The data processing system of Claim ~~12~~ 13, wherein the first and second receivers respectively comprise first and second differential amplifier circuits.

18. (Original) The data processing system of Claim 17, wherein the first differential amplifier circuit is responsive to a first reference voltage and a data signal carried on the second channel line, and wherein the second differential amplifier circuit is responsive to a second reference voltage and a data signal carried on the first channel line.

19. (Original) The data processing system of Claim 17, further comprising:

a first level shifter circuit that couples the second channel line to the first differential amplifier circuit; and

a second level shifter circuit that couples the first channel line to the second differential amplifier circuit.

20. (Currently amended) The data processing system of Claim ~~11~~ 13, wherein a magnitude of the terminal voltage is greater than magnitudes of the memory supply voltage and the controller supply voltage, respectively.

21 – 24. (Canceled)